# Lab N°2

## ATPG, SCAN and TRANSITION FAULTS

Lab Objectives:
- ATPG
- Sequential ATPG
- Scan chain insertion and Scan test

## Exercise 1:

### 1. Lab preparation

Exercise 1 of Lab N°1.

### 2. Lab Practice

Afin d'utiliser l'outil TETRAMAX de Synopsys vous devez lancer la commande (à préciser en salle) afin d'indiquer les chemins relatifs à l'outil. L'outil se lance par la commande tmax &. TETRAMAX se présente sous la forme d'une interface graphique présentée sur la Figure 1.

In order to use Synopsys' TETRAMAX tool, you must launch the command (to be specified during the lab) in order to indicate the paths relating to the tool. The tool is launched by the command tmax &. TETRAMAX comes in the form of a GUI shown in Figure 1.
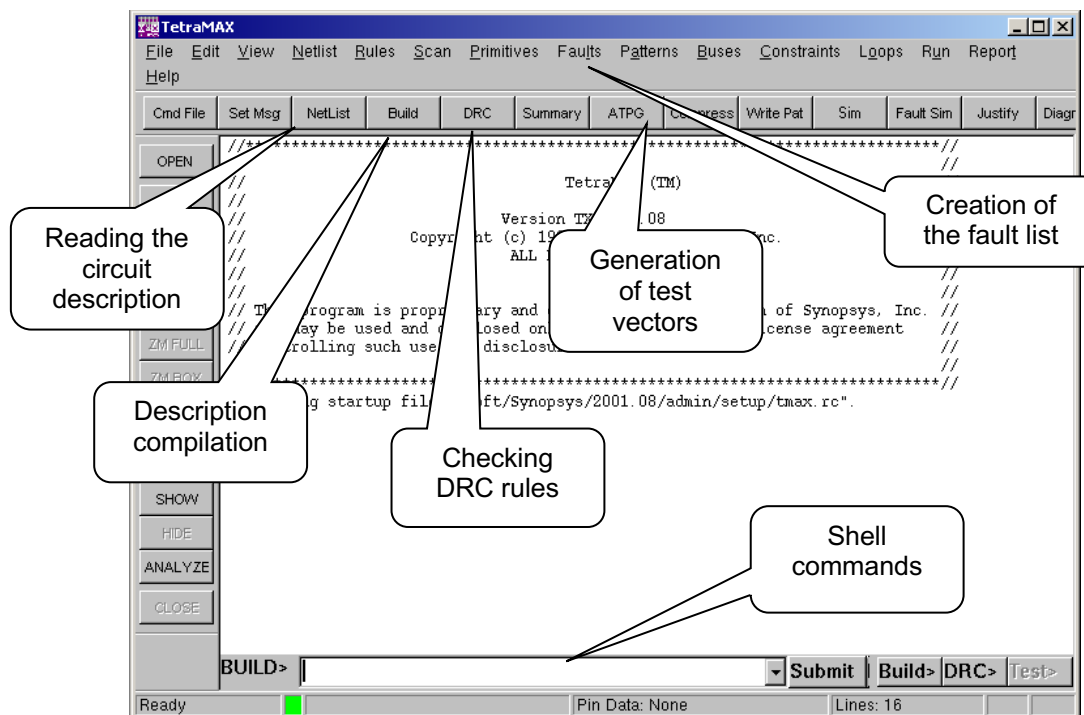


Figure 1: TETRAMAX GUI

The test of the circuit presented above will take place in several phases:

- Preparation of files: You must copy Verilog circuit descriptions and gate libraries.

- Reading the description of the circuit: Using the **NetList** button you obtain the window shown in Figure 2. From this window, you must choose the input files, i.e. the library and the circuit description. First, you must read the **lib_comb.v** file by checking **Library Modules**. This file contains the gates used in the description of the circuit to be tested. Finally, you must again click on **NetList** to read your **Verilog description** without checking **Library Modules**.
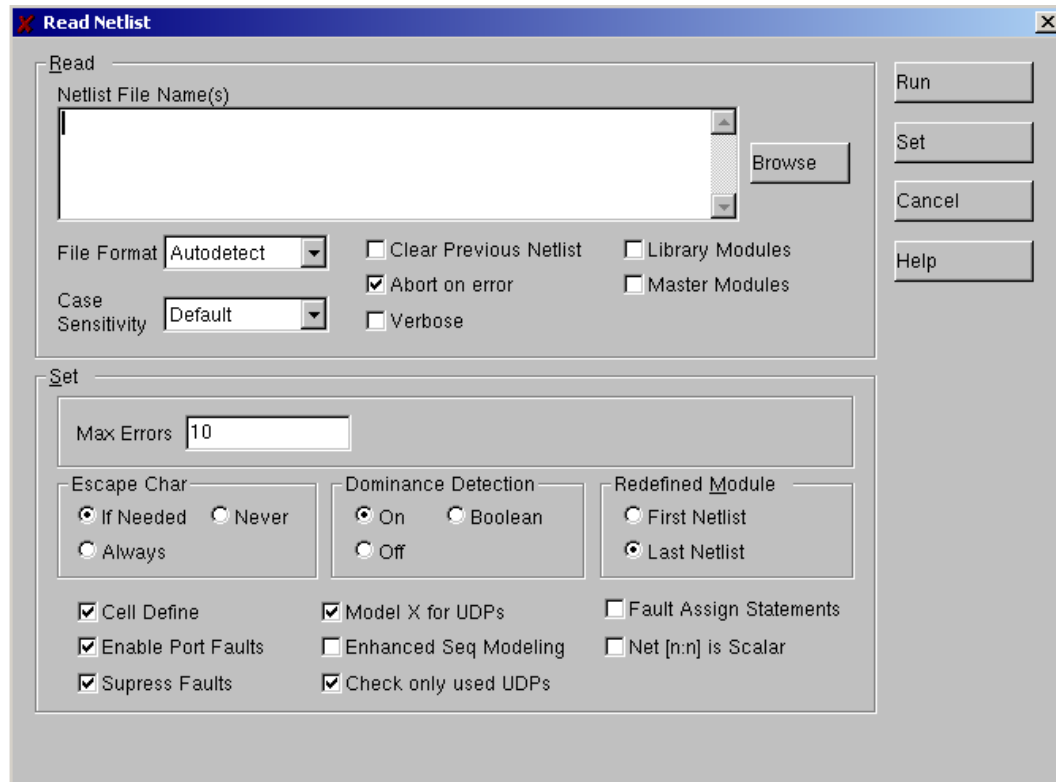


Figure 2: Read Netlist window

- Compilation of the circuit: Click on the button **Built** to launch the compilation of your **Verilog description**. Check that the name entered in **Top Module Name** corresponds to the name of your circuit.
- Checking the DRC rules (Design Rules Checking): This step cannot be considered during this practical work because it uses files generated by other tools upstream in the design flow. Click on **DRC** then **OK** to skip the step to access the test.

From this step, you can visualize the circuit. To do this, click on the **OPEN GSV** button then **SHOW All**.

- Fault model: In the **Faults tab** select **Set Fault Options**, this window (see Figure 3) allows you to select the fault model. Select the **Stuck** model as well as the **Uncollapsed** option in **Report**.
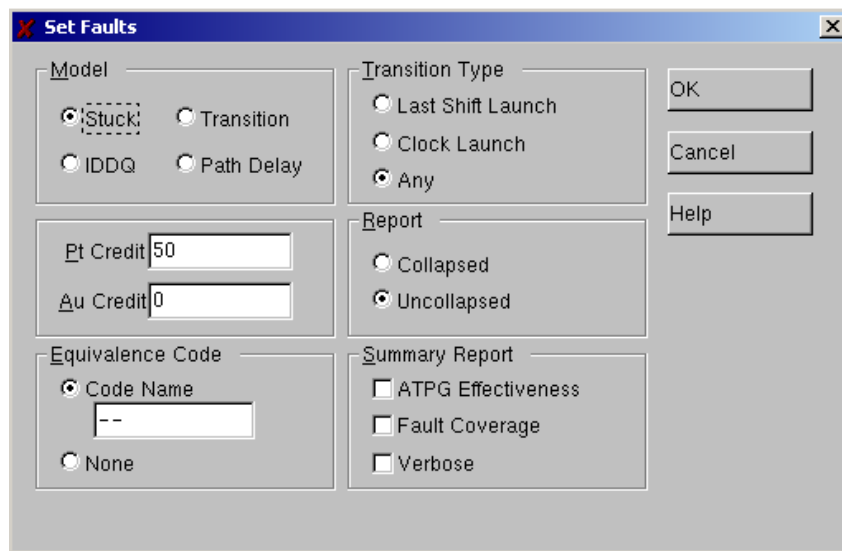
Figure 3: Set Faults window

- Fault list generation: In the **Faults** menu, select **Add Faults**. This option allows you to create a fault list in different ways. The fastest is to choose the **All** option (all faults are considered). The number of faults is displayed on the main window, compare this result to the result obtained in the theoretical part. Still in the **Faults** menu, you can view the fault list with **Report Faults**. **Remove Faults** allows you to delete the fault list. **Repeat** the previous steps with the **Collapsed** option. Compare the results with those of the theoretical part.
- Test vector generation: Use the **ATPG** button which will open the window shown in Figure 4. From the **General ATPG Setting** tab, you can perform the majority of test vector generations. Choose automatic mode by clicking on the **Auto** button. In this case, the generation tool adapts the different constraints in order to obtain a test vector sequence allowing to reach a maximum fault coverage rate. On the main window, you can read the coverage rate and the number of test vectors needed to test your circuit.
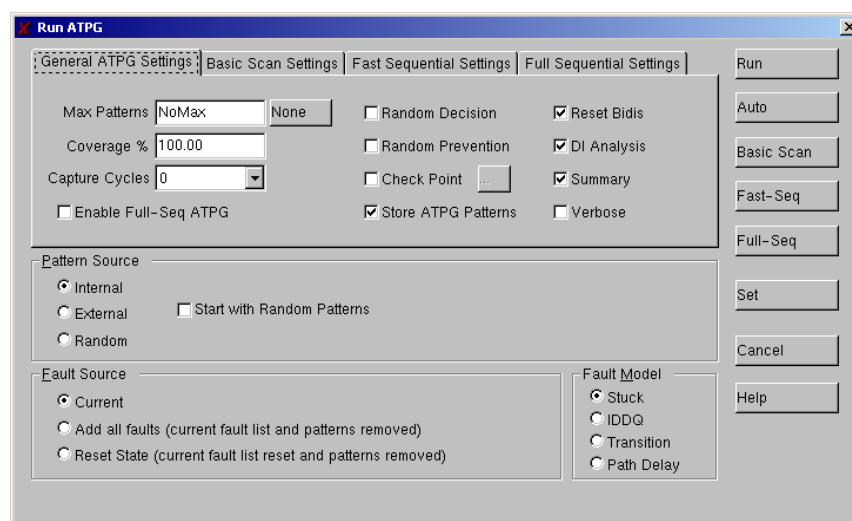


Figure 4: Run ATPG window

- Pattern sequence: In the **Patterns** menu, choose **Report Patterns** to view the list of test vectors (see Figure 5). Verify that you get the same results as the test tool.
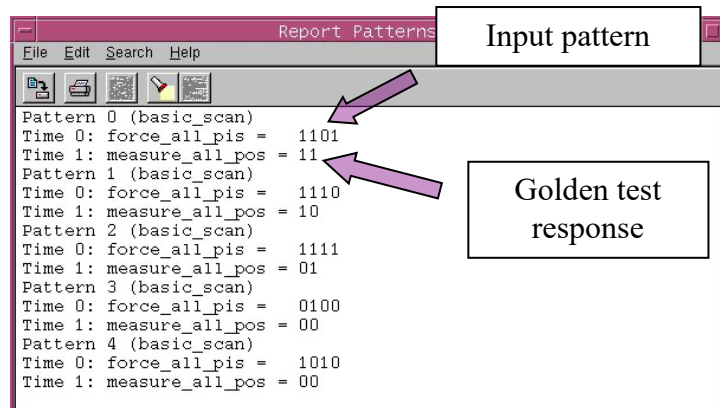


Figure 5: Report pattern window

- Fault effect path analysis: In the left menu click on **ANALYSIS**, then on the **Faults** tab the window (see Figure 6) opens. In this example we want to analyze step by step the test of the sticking at 0 of the B input of gate 3 (gate_3/B Stuck at 0). Click on **OK**, you can see on the main window (Figure 7) the path used by the fault effect and the values to be applied to the inputs of the logic gates to propagate this fault effect.
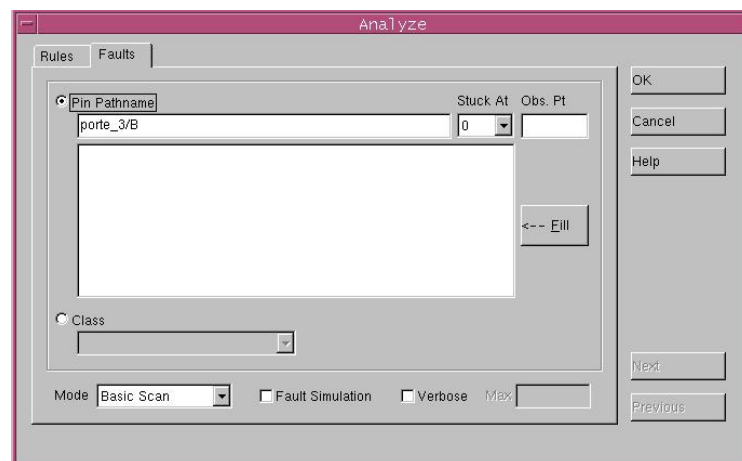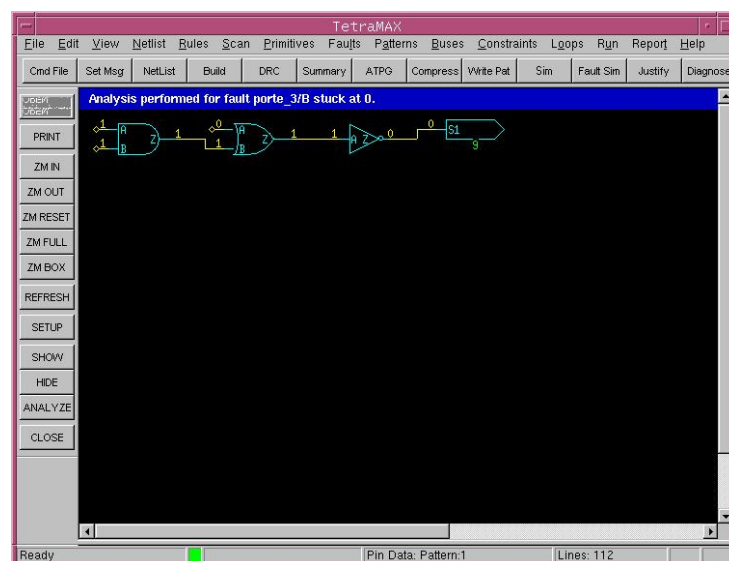


Figure 6: Analyze window



Figure 7: Analyse window

## Exercise 2:

Performed the same process using the circuit presented inf Figure 8.
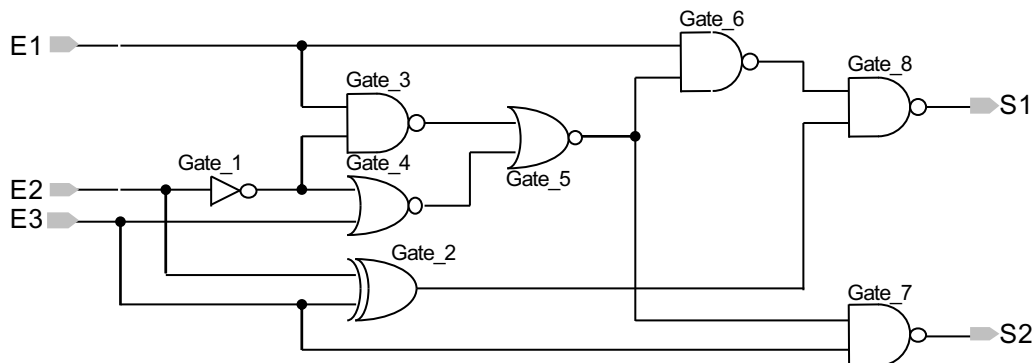


Figure 8: Exercise 2

## Exercise 3: Sequential circuit test

The purpose of testing a sequential circuit is the same as that of a combinatorial circuit, to find the test vectors to verify the circuit. In this part, we will use D flip-flops in sequential circuits. Two techniques will be used for the test: the technique without DfT and the SCAN technique.

In this part, you will need a new library (sequential library). To access this library, copy the lib_seq.v file which is in the same place as the combinatorial library. As in the case of the combinatorial library, you must read the lib_seq.v file using **NetList** and checking **Library Modules**. Also, since the circuit is sequential, hence has a clock, you need to tell the software the name of the clock input. To do this, click on the **Scan** tab then **Clocks** and **Add Clocks**.

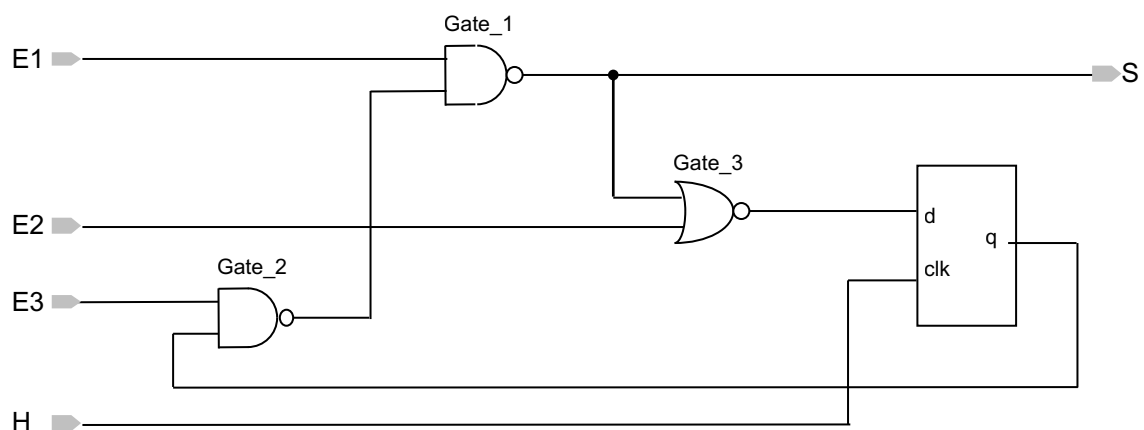Consider as fist case study the sequential circuit depicted in Figure 9.



Figure 9: Exercise 3 sequential circuit

## 3.1 Sequential ATPG

**QUESTIONS:**
- Determine the input stimuli to be applied to test the SA0 of input A of Gate_3. Detail the Sensitisation, Propagation and Justification stages.

Using TETRAMAX :
- As seen previously for the combinatorial circuit, read the two libraries lib_comb.v and lib_seq.v using the **Library Modules** option.
- Read the Verilog description of the circuit.
- Compilation of the circuit with **Built**
- Create the clock with the **Scan** tab (Figure 9)
- DRC rules check with **DRC** button
- Generation of test vectors with the **ATGP** button (select the sequential ATPG engine!!!).

## 3.2 SCAN approach

**QUESTIONS:**
- Draw the circuit scheme so as to use the SCAN technique
- Determine the stimuli to apply to test the SA0 of input A of Gate_3.

Using TETRAMAX:
- Read combinatorial and sequential libraries as well as the circuit description
- Compile the circuit
- Indicate the name of the clock
- Check DRC rules
- Use the **SCAN** menu then **Set Scan Ability**. This option allows you to select the number of FF you want to insert in the Scan chain. This allows you to obtain a partial SCAN or a full SCAN.
- Generate test vectors

## 3.3 Application to circuit s510

The objective of this part of the lab will be to test this circuit using different DfT techniques.
- Test this circuit in its original version, i.e., without using any DfT.
- Turn the flip-flops into a reset flip-flop and test the circuit again.
- Change the flip-flops to a set and reset flip-flop with independent control input per flip-flop and test the circuit again.
- Finally, use the full SCAN technique.